made more consistent.

[0151]

In Embodiment 5, an example was shown in which two types of impurity introduction regions and the positioning mark have been formed with self-alignment, but it is also possible to form three or more types of impurity introduction regions and the positioning mark with self-alignment.

[0152]

[Advantage of the invention]

With the above-described embodiments of the invention, it is possible to provide a method for manufacturing a semiconductor device with which an impurity introduction region and a positioning mark region can be formed that are aligned to one another, based on a common insulating film pattern and without inviting deterioration of the semiconductor device characteristics.

[Brief description of the drawings]

FIGS. 1A to 1D are cross-sectional views illustrating a method for manufacturing a semiconductor device according to Embodiment 1.

FIGS. 2A to 2E are cross-sectional views illustrating the method for manufacturing a semiconductor device according to Embodiment 1.

FIG. 3 is a graph showing the relation between the diffraction efficiency and the level difference formed by the method for manufacturing a semiconductor device according to Embodiment 1.

FIGS. 4A to 4D are cross-sectional views illustrating a method for manufacturing a semiconductor device according to Embodiment 2.

FIGS. 5A to 5D are cross-sectional views illustrating the method for manufacturing a semiconductor device according to Embodiment 2.

FIGS. 6A to 6F are cross-sectional views illustrating a method for manufacturing a semiconductor device according to Embodiment 3.

FIGS. 7A to 7D are cross-sectional views illustrating a method for manufacturing a semiconductor device according to Embodiment 4.

FIGS. 8A to 8D are cross-sectional views illustrating the method for manufacturing a semiconductor device according to Embodiment 4.

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FIGS. 9A to 9E are cross-sectional views illustrating a method for manufacturing a semiconductor device according to Embodiment 5.

FIGS. 10A to 10E are cross-sectional views illustrating the method for manufacturing a semiconductor device according to Embodiment 5.

FIGS. 11A to 11D are cross-sectional views illustrating a